WHAT IS CLAIMED IS:

1. An active pixel sensor for producing images from electron-hole producing radiation comprising:

A) a solid state radiation detection unit comprising:

1) a crystalline semiconductor substrate;

2) a plurality of Complementary Metal Oxide Semiconductor pixel circuits incorporated into said substrate to form an array of pixel circuits, wherein each of said array of pixel circuits comprises:

a) a charge collecting pixel electrode;

b) a charge sensing node;

c) a gate bias transistor separating said charge collecting pixel electrode and said charge sensing node;

d) a pixel capacitor comprising said charge collecting pixel electrode and said charge sensing node, wherein said pixel capacitor is configured to store charges collected by said charge collecting pixel electrode;

e) a charge measuring circuit comprising at least one transistor, wherein a gate of said at least one transistor is electrically connected to said charge sensing node;

3) a radiation absorbing layer comprised of photoconductive material covering at least a portion of said array of pixel circuits, wherein said photoconductive material is photoconductive on exposure

to said electron-hole producing radiation;

4) a surface electrode layer comprised of electrically conducting material and formed on said radiation absorbing layer, wherein said surface electrode layer is at least partially transparent to said electron-hole producing radiation, and connected to a voltage source for establishing an electrical field across said radiation absorbing layer and between said surface electrode layer and each of said array of charge collecting pixel electrodes; and

B) an array measurement circuit for measuring charges collected by each of said array of charge collecting pixel electrodes, and for outputting pixel data indicative of said collected charges, wherein said pixel data comprises information defining an image.

2. The sensor according to claim 1, wherein each of said array of pixel electrodes are maintained at substantially equal potential by said gate bias transistor.

3. The sensor according to claim 1, wherein a gate of said gate bias transistor is biased by constant voltage to minimize pixel crosstalk among adjacent pixel electrodes within said array of pixel electrodes.

4. The sensor according to claim 1, wherein said charge sensing node comprises metal and provides an electrical connection to said gate of said at least one transistor in said charge measuring circuit.

5. The sensor according to claim 1, wherein said charge sensing node comprises polycrystalline semiconductor material and provides an electrical connection to said gate of said at least one transistor in said charge measuring circuit.

6. The sensor according to claim 1, wherein said charge sensing node comprises a p-type doped region in said substrate and provides an electrical connection to said gate of said at least one transistor in said charge measuring circuits.

7. The sensor according to claim 1, wherein said charge sensing node comprises a n-type doped region in said substrate and provides an electrical connection to said gate of said at least one transistor in said charge measuring circuits.

8. The sensor according to claim 1, wherein each of said array of pixel circuits comprises at least two transistors.

9. The sensor according to claim 1, wherein each of said array of pixel circuits comprises at least four transistors.

10. The sensor according to claim 1, wherein each of said array of pixel circuits comprises at least six transistors.

11. The sensor according to claim 1, wherein said pixel capacitor is defined by the structure between said charge sensing node and said crystalline semiconductor substrate.

12. The sensor according to claim 1, wherein said radiation absorbing layer comprises hydrogenated amorphous silicon.

13. The sensor according to claim 1, wherein said radiation absorbing layer is a continuous layer.

14. The sensor according to claim 1, wherein said radiation absorbing layer is a discontinuous layer.

15. The sensor according to claim 1, wherein said radiation absorbing layer is a patterned layer.

16. The sensor according to claim 1, wherein said radiation absorbing layer comprises trenches.

17. The sensor according to claim 1, wherein said radiation absorbing layer is substantially planar.

18. The sensor according to claim 1, wherein said radiation absorbing layer is a continuous layer that is fabricated during a continuous deposition process.

19. The sensor according to claim 1, wherein said radiation absorbing layer is a p-n photodiode layered structure, wherein said p-layer is electrically connected to said charge collecting pixel electrode, and said n-layer is electrically connected to said surface electrode layer.

20. The sensor according to claim 1, wherein said radiation absorbing layer is a p-I-n photodiode layered structure, wherein said n-layer is electrically connected to said charge collecting pixel electrode, and said p-layer is electrically connected to said surface electrode layer.

21. The sensor according to claim 20, wherein said p-layer comprises p-type doped hydrogenated amorphous silicon.

22. The sensor according to claim 20, wherein said n-layer comprises n-type doped hydrogenated amorphous silicon.

23. The sensor according to claim 20, wherein said I-layer comprises un-intentionally doped hydrogenated amorphous silicon.

24. The sensor according to claim 1, wherein said radiation absorbing layer is a n-I-p photodiode layered structure, wherein said p-layer is electrically connected to said charge collecting pixel electrode, and said n-layer is electrically connected to said surface electrode layer.

25. The sensor according to claim 24, wherein said p-layer comprises p-type doped hydrogenated amorphous silicon.

26. The sensor according to claim 24, wherein said n-layer comprises n-type doped hydrogenated amorphous silicon.

27. The sensor according to claim 24, wherein said I-layer comprises un-intentionally doped hydrogenated amorphous silicon.

28. The sensor according to claim 1, wherein said radiation absorbing layer comprises a photoconductive un-intentionally doped layer.

29. The sensor according to claim 28, wherein said photoconductive un-
2 intentionally doped layer comprises hydrogenated amorphous silicon.

30. The sensor according to claim 1, wherein said charge collecting pixel
2 electrode comprises a patterned metal plate.

31. The sensor according to claim 1, wherein said charge collecting pixel
2 electrode is formed by a surface of at least one via used for interlayer connection by a semiconductor fabrication process.

32. The sensor according to claim 1, wherein said charge collecting pixel
2 electrode is formed by a surface of a single via.

33. The sensor according to claim 1, wherein said surface electrode layer
2 comprises indium tin oxide.

34. The sensor according to claim 1, wherein said surface electrode layer
2 comprises tin oxide.

35. The sensor according to claim 1, wherein said surface electrode layer
2 comprises titanium nitride.

36. The sensor according to claim 1, wherein a potential difference between adjacent pixel electrodes is in a range of about 1 to about 50 millivolts.

37. The sensor according to claim 1, wherein said sensor comprises a fill factor of at least 40 percent.

38. The sensor according to claim 1, wherein said sensor comprises a fill factor of at least 80 percent.

39. A method of minimizing pixel crosstalk between pixels in an active pixel sensor array comprising:

A) fabricating a solid state radiation detection unit comprising:

1) providing a crystalline semiconductor substrate;

2) incorporating a plurality of Complementary Metal Oxide Semiconductor pixel circuits into said substrate to form an array of pixel circuits, wherein each of said array of pixel circuits comprises:

a) a charge collecting pixel electrode;

b) a charge sensing node;

c) a gate bias transistor separating said charge collecting pixel electrode and said charge sensing node;

d) a pixel capacitor comprising said charge collecting pixel

electrode and said charge sensing node, wherein said pixel capacitor is configured to store charges collected by said charge collecting pixel electrode;

e) a charge measuring circuit comprising at least one transistor, wherein a gate of said at least one transistor is electrically connected to said charge sensing node;

3) covering at least a portion of said array of pixel circuits with a radiation absorbing layer comprising photoconductive material, wherein said photoconductive material is photoconductive on exposure to said electron-hole producing radiation;

4) forming a surface electrode layer comprising electrically conducting material on said radiation absorbing layer, wherein said surface electrode layer is at least partially transparent to said electron-hole producing radiation, and connected to a voltage source for establishing an electrical field across said radiation absorbing layer and between said surface electrode layer and each of said array of charge collecting pixel electrodes;

B) measuring charges collected by each of said array of charge collecting pixel electrodes with an array measurement circuit; and

C) outputting pixel data indicative of said collected charges of said array of charge collecting pixel electrodes, wherein said pixel data comprises information defining an image.

40. The method according to claim 39, wherein each of said array of pixel electrodes are maintained at substantially equal potential by said gate bias transistor.

41. The method according to claim 39, wherein a gate of said gate bias transistor is biased by constant voltage to minimize pixel crosstalk among adjacent pixel electrodes within said array of pixel electrodes.

42. The method according to claim 39, wherein said charge sensing node comprises metal and provides an electrical connection to said gate of said at least one transistor in said charge measuring circuit.

43. The method according to claim 39, wherein said charge sensing node comprises polycrystalline semiconductor material and provides an electrical connection to said gate of said at least one transistor in said charge measuring circuit.

44. The method according to claim 39, wherein said charge sensing node comprises a p-type doped region in said substrate and provides an electrical connection to said gate of said at least one transistor in said charge measuring circuits.

45. The method according to claim 39, wherein said charge sensing node comprises a n-type doped region in said substrate and provides an electrical connection to said gate of said at least one transistor in said charge measuring circuits.

46. The method according to claim 39, wherein each of said array of pixel circuits comprises at least two transistors.

47. The method according to claim 39, wherein each of said array of pixel circuits comprises at least four transistors.

48. The method according to claim 39, wherein each of said array of pixel circuits comprises at least six transistors.

49. The method according to claim 39, wherein said pixel capacitor is defined by the structure between said charge sensing node and said crystalline semiconductor substrate.

50. The method according to claim 39, wherein said radiation absorbing layer comprises hydrogenated amorphous silicon.

51. The method according to claim 39, wherein said radiation absorbing layer is a continuous layer.

52. The method according to claim 39, wherein said radiation absorbing layer is a discontinuous layer.

53. The method according to claim 39, wherein said radiation absorbing layer is a patterned layer.

54. The method according to claim 39, wherein said radiation absorbing layer comprises trenches.

55. The method according to claim 39, wherein said radiation absorbing layer is substantially planar.

56. The method according to claim 39, wherein said radiation absorbing layer is a continuous layer that is fabricated during a continuous deposition process.

57. The method according to claim 39, wherein said radiation absorbing layer is a p-n photodiode layered structure, wherein said p-layer is electrically connected to said charge collecting pixel electrode, and said n-layer is electrically connected to said surface electrode layer.

58. The method according to claim 39, wherein said radiation absorbing layer is a p-I-n photodiode layered structure, wherein said n-layer is electrically connected to said charge collecting pixel electrode, and said p-layer is electrically connected to said surface electrode layer.

59. The method according to claim 58, wherein said p-layer comprises p-type doped hydrogenated amorphous silicon.

60. The method according to claim 58, wherein said n-layer comprises n-type doped hydrogenated amorphous silicon.

61. The method according to claim 58, wherein said I-layer comprises un-intentionally doped hydrogenated amorphous silicon.

62. The method according to claim 39, wherein said radiation absorbing layer is a n-I-p photodiode layered structure, wherein said p-layer is electrically connected to said charge collecting pixel electrode, and said n-layer is electrically connected to said surface electrode layer.

63. The method according to claim 62, wherein said p-layer comprises p-type doped hydrogenated amorphous silicon.

64. The method according to claim 62, wherein said n-layer comprises n-type doped hydrogenated amorphous silicon.

65. The method according to claim 62, wherein said I-layer comprises un-intentionally doped hydrogenated amorphous silicon.

66. The method according to claim 39, wherein said radiation absorbing layer comprises a photoconductive un-intentionally doped layer.

67. The method according to claim 66, wherein said photoconductive un-intentionally doped layer comprises hydrogenated amorphous silicon.

68. The method according to claim 39, wherein said charge collecting pixel electrode comprises a patterned metal plate.

69. The method according to claim 39, wherein said charge collecting pixel electrode is formed by a surface of at least one via used for interlayer connection by a semiconductor fabrication process.

70. The method according to claim 39, wherein said charge collecting pixel electrode is formed by a surface of a single via.

71. The method according to claim 39, wherein said surface electrode layer comprises indium tin oxide.

72. The method according to claim 39, wherein said surface electrode layer comprises tin oxide.

73. The method according to claim 39, wherein said surface electrode layer comprises titanium nitride.

74. The method according to claim 39, wherein a potential difference between adjacent pixel electrodes is in a range of about 1 to about 50 millivolts.

75. The method according to claim 39, wherein said sensor comprises a fill factor of at least 40 percent.

76. The method according to claim 39, wherein said sensor comprises a fill factor of at least 80 percent.